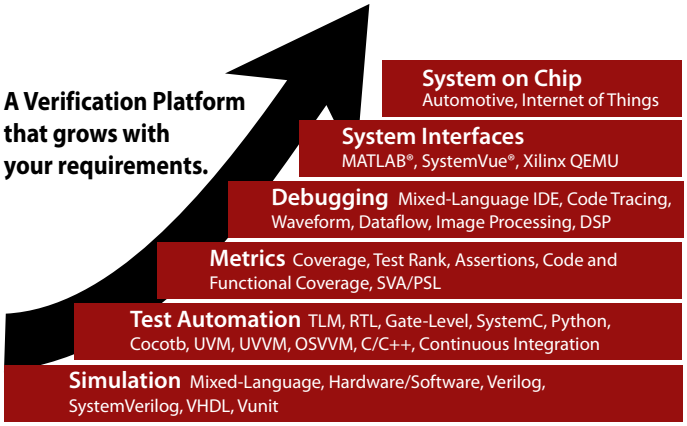
Riviera-PRO™ | Advanced Verification

Verification Platform

Riviera-PRO™ addresses verification needs of engineers crafting tomorrow's cutting-edge FPGA and SoC devices. Riviera-PRO enables the ultimate testbench productivity, reusability, and automation by combining the high-performance simulation engine, advanced debugging capabilities at different levels of abstraction, and support for the latest Language and Verification Library Standards.



Top Benefits

- **Standards-based support for VHDL, SystemVerilog, and SystemC to enable design and verification of the most sophisticated digital designs**
- **High-performance simulator with industry-leading capacity and high regression throughput for developing complex systems**
- **Integrated multi-language debug environment to automate time-consuming design analysis tasks and fix bugs quickly**
- **Comprehensive assertion-based verification (SVA, PSL) for increased design observability and decreased debug time**
- **Advanced code coverage capabilities and coverage analysis tools for fast metric-based verification closure**
- **Supports methodologies like UVM, OS-VVM, UVVM, Cocotb, and Vunit for advanced verification strategies.**

High Performance Simulation

Riviera-PRO incorporates industry-leading simulation optimization algorithms to achieve the highest performance in mixed-language simulations. Combined with the industry-leading capacity, Riviera-PRO enables high regression throughput for developing the most complex systems.

Advanced Debugging

Integrated multi-language debug environment enables automating time-consuming design analysis tasks and fixing bugs quickly. It supports all standard languages and provides intuitive ways to visualize and analyze key objects in your design. Built-in debugging tools provide code tracing, waveform, dataflow, coverage, assertion, UVM, and memory visualization capabilities.

Industry's Best ROI

Riviera-PRO enables Aldec customers to deliver innovative products at a lower cost in shorter time. Aldec's proven design automation methods help customers to speed up the design and implementation of products for automotive, medical, aerospace, and military applications. In addition to EDA tool packages accompanied by the comprehensive trainings and support, Aldec invests in the partnerships and integrations necessary to build complete design and verification flows.

STANDARDS

SILICON

INTERFACES

FEATURES	PRODUCT CONFIGURATIONS		
Supported Standards	LV	LVT	LVT-SV
VHDL IEEE 1076 (1987, 1993, 2002, 2008, and 2019)	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•
SystemVerilog IEEE 1800™-2012 (Design)	•	•	•
SystemC™ 2.3.1 IEEE 1666™/TLM 2.0	Option	•	•
SystemVerilog IEEE 1800™ 2012 (Verification)	--	--	•
Verification Libraries (OSVVM, UVVM)	•	•	•
Universal Verification Methodology (UVM)	--	--	•
Design Entry and Design Management			
HDL Editor with Auto-Complete and Code Templates	•	•	•
UVM Generator & Register Model Generator	•	•	•
Design and Library Managers, File Browser	•	•	•
Customizable GUI Perspectives	•	•	•
Task Management	•	•	•
Macro, Tcl/Tk, Perl script support	•	•	•
Debug and Analysis			
Interactive Code Execution Tracing	•	•	•
Advanced Breakpoint Management	•	•	•
Accelerated Waveform Viewer (ASDB)	•	•	•
Post-Simulation Debug	•	•	•
Waveform Compare	•	•	•
Plot Window & Image Viewer	•	•	•
FSM Debug/FSM Toolbox	•	•	•
Assertions in Waveform and Debugging	Option	•	•
Integrated C/SystemC Debugger	--	•	•
X-Trace	Option	•	•
Dataflow	Option	•	•
Classes Window	--	--	•
UVM Graph & Toolbox	--	--	•
Simulation/Verification			
Single or Mixed Language	•	•	•
Verilog Programming Language Interfaces (PLI/VPI)	•	•	•
VHDL Procedural Interface (VHPI)	•	•	•
SystemVerilog IEEE 1800™ DPI 2.0	•	•	•
Value Change Dump (VCD and Extended VCD) Support	•	•	•
Incremental Compilation	•	•	•
Multi-Threaded Compilation	•	•	•
Simulation Model Protection/Library Encryption	•	•	•
IEEE 1735™ Interoperable Encryption	•	•	•
Xilinx® SecureIP Support	Option	•	•
Intel® FPGA Language-Neutral Libraries	Option	•	•
Simulation Performance Optimization (Verilog/SystemVerilog, VHDL)	--	•	•
64-bit Simulation	•	•	•
Transaction-Level Visual Debugging	--	Option	•
SFM (Server Farm Manager)	Option	Option	•
HES™ Hardware Assisted Verification (Acceleration and Emulation)	Option	Option	Option
Assertions and Coverage Tools			
PSL, SystemVerilog Assertions and Functional Coverage (Assertion)	Option	•	•
Code and Toggle Coverage and UCIS-compatible Aldec Coverage Database	Option	•	•
Functional Coverage (OSVVM)	Option	•	•
Functional Coverage (SV Coverage)	--	--	•
External Simulation Interfaces			
Synopsys® SmartModels, SWIFT Interface and LMTV	Option	•	•
Synopsys® Verdi™ FSDB Recording	Option	•	•
Co-Simulation Interfaces			
Agilent SystemVue®	•	•	•
MathWorks Simulink®	•	•	•
MathWorks MATLAB®	Option	•	•
Aldec QEMU Bridge (Linux Only)	Option	•	•
Design Rule Checking			
ALINT-PRO™ with Aldec Basic Rule Library	Option	•	•
DO-254 VHDL or Verilog Rule Library	Option	Option	Option
STARC® VHDL or Verilog Rule Library	Option	Option	Option
Reuse Methodology Manual (RMM) Rule Library	Option	Option	Option
Supported Platforms			
Windows® 11/10/Server 2022, 2019, 2016, 2012 (64 bit)	•	•	•
Linux (64 bit)	•	•	•

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THE DESIGN VERIFICATION COMPANY