Static Design Verification

ALINT-PRO™ is a static design verification solution for VHDL, Verilog, and SystemVerilog designs that uncovers critical design issues early in the design cycle without involving simulation. Running ALINT-PRO before RTL simulation and logic synthesis phases prevents design issues from spreading into the downstream stages of design flow and reduces the number of iterations required to finish the design.

ALINT-PRO™ covers a wide range of design issues including RTL and post-synthesis simulation mismatches, FSM checks, clock and reset trees analysis, clock and reset domain crossings, design partitioning, DFT, coding for reuse and portability, and many more.

Key Benefits/Top Features

- **Static Design Verification** – performs analysis based on RTL and SDC sources without requiring complicated setup

- **DO-254 Support** – includes a dedicated ruleset for safety critical designs to achieve compliance with DO-254 guidelines

- **RISC-V Support** – includes a ruleset implementing industry-best practices and guidelines for the RISC-V design community.

- **Schematic Visualization** – for efficient issues analysis, violated paths representation in graphical form, and clock domains highlight

- **CDC and RDC Verification** – obtain all RTL and CDC/RDC checks in the same product with the ALDEC_CDC rule plug-in, providing the best possible linting results

- **FPGA Vendors Support** – automated conversion of FPGA vendors projects to ALINT-PRO environment and full FPGA vendors libraries support

- **Design Constraints** – easy design setup (reuse of existing constraints) facilitates initial design constraints creation

- **Design Constraints Extension** – increase analysis quality by proper verification of IPs, behavioral modules, and black boxes

Industry Proven Guidelines

ALINT-PRO supports rule checks based on STARC (Semiconductor Technology Academic Research Center) and RMM (Reuse Methodology Manual) guidelines to utilize best practices in design development used by major semiconductor companies.

For safety critical designs, ALDEC offers the DO-254 rule plug-in, focused on design stability, and is recommended to help achieve design compliance with the DO-254 standard. For RISC-V Design Community, ALDEC offers the RISC-V rule plugin, based on the industry-proven best IP design practices and guidelines.
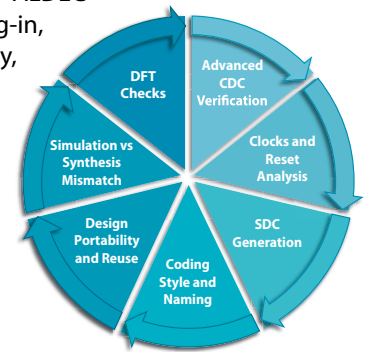
ALDEC Basic and Premium rule plug-ins capture the combined knowledge of Aldec customers as well as in-house design experts and can supplement the above plug-ins, while the ALDEC SV plug-in targets new varieties of RTL mistakes specific to SystemVerilog design subsets.

ALINT-PRO contains a powerful Policy Editor to quickly build an efficient rules configuration based on design needs.

CDC and RDC Verification

ALINT-PRO features an optional ALDEC_CDC rule plug-in, which enables the full power of Clock and Reset Domain Crossing (CDC, RDC) with RTL analysis in a single product. It enhances verification with dynamic checks based on assertions and metastability emulation, and offers additional debug capabilities such as schematic highlight of clock and reset domains, and browsing the detected domain crossings and identified synchronizers.

FPGA Vendors Support

ALINT-PRO supports an automated FPGA Projects conversion for Xilinx, Intel FPGA and Microchip. Also, Alint-PRO contains precompiled and constrained FPGA vendors libraries to be used for Advanced Linting and CDC/RDC analysis.

ALDEC
THE DESIGN VERIFICATION COMPANY

FEATURES	PRODUCT CONFIGURATIONS
Supported Standards	
Verilog® IEEE 1364 (1995, and 2001)	•
SystemVerilog® IEEE 1800 (2005 and 2009)	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•
Rule Libraries	
ALDEC BASIC (VHDL and Verilog)	•
ALDEC PREMIUM (VHDL and Verilog)	ALDEC PREMIUM Option
ALDEC SV (SystemVerilog Design subset)	ALDEC SV Option
STARC (VHDL and Verilog)	STARC VHDL/VLOG Option
DO254 (VHDL and Verilog)	DO254 VHDL/VLOG Option
RMM (VHDL and Verilog)	RMM VHDL/VLOG Option
RISCV (Verilog and SystemVerilog)	RISCV Option
ALDEC CDC (VHDL, Verilog, and SystemVerilog)	ALDEC CDC Option
Core Mechanisms	
Clocks and Resets Auto-detection	•
Clock Domains and Asynchronous Clock Groups Extraction	•
Metastability Insertion for CDC-aware Simulation	ALDEC CDC Option
CDC Assertions and Coverage Statements for Crossings	ALDEC CDC Option
Reset Domains Extraction and RDC Verification	ALDEC CDC Option
Multi-mode CDC analysis (Consolidated, Case-based)	ALDEC CDC Option
Reading and Generating SDC Constraints	•
Incremental Design Entry and Hierarchical Constraints Promotion	•
FPGA Vendor Library Components Support (Xilinx, Intel, Microchip, Lattice)	•
Extracting Finite State Machines from RTL	•
Unit and Full Mode Linting	•
DFT Checks	STARC VHDL/VLOG Option
Debug Capabilities	
RTL Schematic Viewer and Control Schematics	Schematics Option
Clocks and Resets Viewer	•
FSM Viewer and FSM Graph	•
Library Viewer and Elaboration Viewer	•
Violation Viewer and Tasks Management	•
Exporting Violation Reports (TXT, CSV, HTML, PDF)	•
CDC Viewer and RDC Viewer	ALDEC CDC Option
CDC Schematics	ALDEC CDC + Schematics Option
Design Management	
Project Manager and File Browser	•
Flow Manager and Phase-based CDC Flow	•
Policy and Waiver Editors	•
Importing Active-HDL, Riviera-PRO, Vivado, ISE, and Quartus Projects	•
Supported Platforms	
Windows® 10/8.1/8/7 32/64 bit	•
Linux 32/64 bit	•

STANDARDS

IEEE

STARC

PARTNERS

Achronix — Data Acceleration

ALTERA now part of Intel

LATTICE SEMICONDUCTOR

MICROCHIP

AMD XILINX

Design Constraints Setup

ALINT-PRO can read existing SDC™ constraint files previously created for synthesis and static timing analysis tools. The tool can also automatically generate initial SDC templates based on the topological analysis, including definitions of master and generated clocks, I/O delays, and asynchronous clock groups.

Design Constraints Extension

ALINT-PRO offers a custom extension to design constraints, an easy to read and straightforward format of block-level constraints to describe non-synthesizable behavioral modules, IP modules with protected code, vendor library cells, etc. Using constraints to describe a module's interface substitutes the black boxes in the netlist with equivalent models, which enable precise linting. It is also possible to describe designer's intent on reset controls, custom synchronization cells, and safe CDC paths, including paths with quasi-static sources.

Framework

ALINT-PRO provides a tightly integrated GUI framework with intuitive interface and efficient issues analysis means. The Framework includes many views:

Schematic Viewer – offers graphical representation of fully synthesized netlists as well as clock domains and violated paths highlighting. Control Schematics graphically demonstrate the relations between clocks and resets. CDC Schematics is a specialized visualization for domain crossings and synchronizers;

Clocks and Resets Viewer – shows clock and reset networks with all pins and nets which they propagate through;

Violation Viewer – enables violations filtering by various criteria, adding waivers, cross-probing to HDL and Schematic, and gives access to summary data.

Active-HDL™, Riviera-PRO™, Vivado™, and Quartus™ projects can be automatically converted to ALINT-PRO format, significantly minimizing design setup time.

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