The Creonic CCSDS 231.0 LDPC IP supports the LDPC coding schemes as defined by the CCSDS standard. The LDPC codes with rate 1/2, coded block lengths 128 and 512 are specially designed for telecommand applications, but the excellent error correction performance makes it the ideal fit for further applications with highest demands on forward error correction. The IP cores are available for ASIC and FPGAs (AMD Xilinx, Intel, Microchip).

CCSDS 231.0 LDPC Decoder

Key benefits of the decoder are:

- Gains of up to 3 dB compared to Viterbi decoders.

- Low-power and low-complexity design.

- Layered LDPC decoder architecture, for convergence behavior that is twice as fast as non-layered LDPC decoders

- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.

- Optional fixed number of iterations for fixed latency of blocks with the same code rate and block length.

- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.

- Collection of statistic information (number of iterations, decoding success, number of modified bits).

CCSDS 231.0 LDPC Encoder

Key benefits of the encoder are:

- High-throughput, low-latency encoder core.

- Low-power and low-complexity design.

Performance Figures

- Encoder air throughput throughput of up to 200 Mbit/s at 200 MHz

- Decoder payload throughput of up to 25 Mbit/s (20 iterations, 200 MHz)

Features

- Support for code rate 1/2

- Uncoded block sizes of 64 and 256 bits

- Compliant with "TC synchronization and channel coding, Recommended Standard, CCSDS 231.0-B-3, Blue Book, September 2017".

Applications

- Telecommand communication.

- Free space optical (FSO) communication.

- Further applications with the highest demands on forward error correction

Deliverables

- VHDL source code or synthesized netlist

- HDL simulation models e.g. for Aldec's Riviera-PRO

- VHDL testbench

- bit-accurate Matlab, C or C++ simulation model

- comprehensive documentation

Error Correction Performance

The following table shows bit error rate (BER) and block error rate (BLER) of the CCSDS 231.0 LDPC decoder.

Code Rate	Block length (k)	E_b/N_0 (dB) at		
		BER 10^{-6}	BER 10^{-7}	BLER 10^{-5}
1/2	64	5.15	5.60	5.20
1/2	256	3.65	3.85	3.65

Error correction performance of the CCSDS 231.0 decoder at 31 iterations and 6 bit input.

Related Products

CCSDS LDPC Decoder and Encoder

CCSDS AR4JA LDPC Decoder and Encoder

CCSDS SCCC Turbo Encoder and Decoder

DVB-S2X LDPC/BCH Decoder

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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