Creonic provides IP cores for CCSDS modulation, SCCC encoding and decoding as well as demodulation.

CCSDS 131.2 Wideband Modulator

The Creonic CCSDS high performance modulator performs all tasks of an inner transmitter. The modulator expects SCCC (Serial Concatenated Convolutional Code) encoded frames as input and performs mapping, Physical Layer (PL) framing and modulation. In addition, the core performs baseband interpolation and output gain adjustment. The output of the core is designed to be followed by a DAC and RF front end.

Benefits

- Easy-to-use mode adaptation input interface.
- Provides interpolated and gain-adjusted ZF baseband signal.
- The modulator contains bit mapping, PL signaling, pilot insertion, PL scrambling, interpolation, baseband filtering and gain adjustment.
- Low-power and low-complexity design.
- Memory-mapped interface for controlling and for retrieving status information.
- Flexible output interface, which can be driven by an external clock for easy synchronization with DAC.
- AXI4-Stream handshaking interfaces for seamless integration.
- Perfectly fits to the Creonic CCSDS SCCC Turbo Encoder.
- Available for ASIC and FPGAs (AMD Xilinx, Intel, Microchip).

Key Features

- Symbol rate of up to 1.2 GSymb/s at 600 MHz.

Features

- Compliant with CCSDS 131.2-B-1
- Supports ACM mode
- Supports roll-off factors 5%, 10%, 15%, 20%, 25% to 35%
- Support for blocks with pilots only
- Support for QPSK to 64-APSK.

Applications

- Satellite communication
  - High data rate telemetry applications
  - Earth Exploration Satellite Service (EESS)
- Applications with the highest demands on forward error correction
- Applications with the need for a wide range of code rates and block lengths

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models
- Bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

The following figure gives an overview of all components that are part of the CCSDS 131.2 Wideband Modulator IP core.

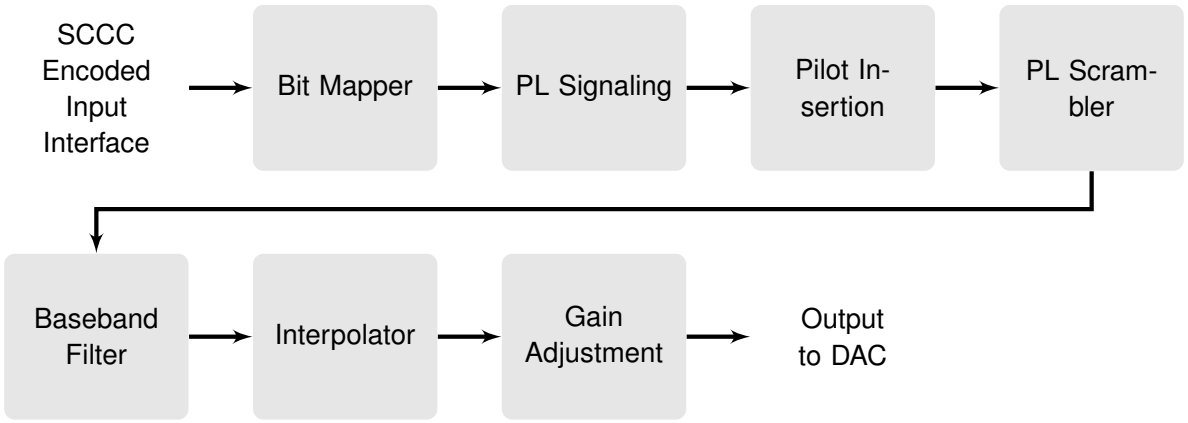


Figure 0.1: Creonic CCSDS Wideband Modulator IP building blocks.

The Creonic CCSDS high performance wideband demodulator performs all tasks of an inner receiver. It allows for processing symbol rates of 500 Msymb/s on state-of-the-art FPGAs.

The demodulator expects the quantized, complex baseband samples from an analog-digital-converter (ADC) and recovers timing, frequency and phase of the complex mapped symbols. In addition, the core handles PL frame recovery and PL deframing. The output interface of the demodulator perfectly fits the Creonic CCSDS forward error correction IP core that implements a Serial Concatenated Convolutional Code (SCCC) decoding.

Benefits

- Contains radio interface, decimator, timing recovery, equalizer, frame acquisition, and carrier recovery.
- Performs and supports DC offset correction, I/Q imbalance correction (optional), decimation (optional), FFT-based blind frequency estimation, coarse frequency estimation, timing recovery, matched filtering, downsampling, frame synchronization, fine frequency correction, coarse and fine phase correction, equalization, PL descrambling, and PL deframing.
- Low-power and low-complexity design.
- On-the-fly configuration.
- Memory mapped interface for controlling the core and for retrieving status information.
- Very fast synchronization due to different sets of filter coefficients for acquisition and tracking mode.
- Configurable interrupts and output of synchronization status information.
- AXI4-Stream handshaking interfaces for seamless integration.
- Perfectly fits to the Creonic CCSDS SCCC Turbo decoder.
- Available for ASIC and FPGAs (AMD Xilinx, Intel).

Features

- Compliant with CCSDS 131.2-B-1
- Supports ACM mode
- Supports roll-off factors 5%, 10%, 15%, 20%, 25% and 35%
- Support for blocks with pilots only
- Support for QPSK to 64-APSK.
- Output of XFECFRAMEs for further processing by the Creonic FEC decoder.

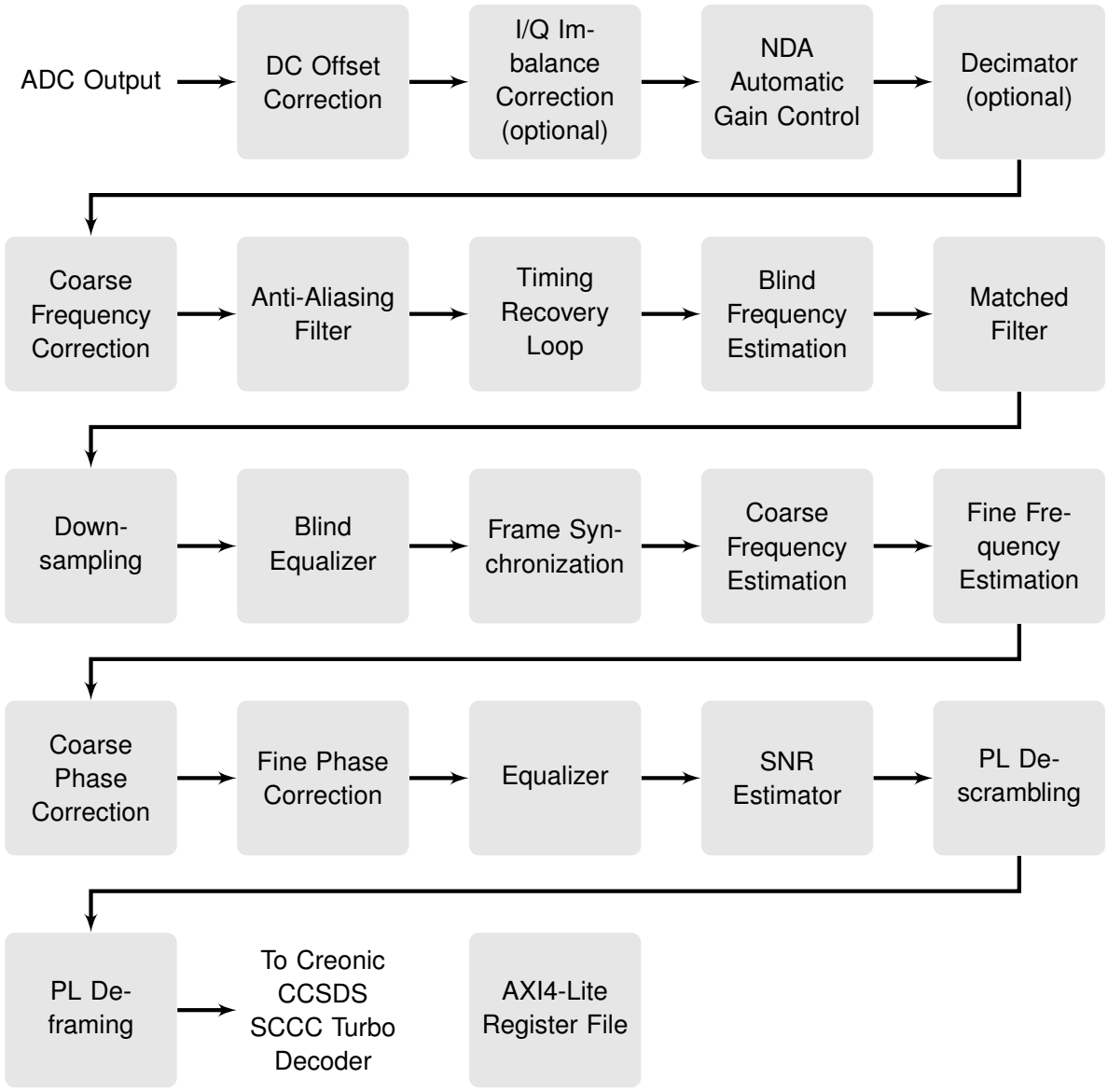
Applications

- Satellite communication
  - High data rate telemetry applications
  - Earth Exploration Satellite Service (EESS)
- Applications with the highest demands on forward error correction
- Applications with the need for a wide range of code rates and block lengths

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models
- Bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

The following figure gives an overview of all components that are part of the CCSDS wideband demodulator IP core:



Related Products

CCSDS 131.2 SCCC Turbo Encoder and Decoder

CCSDS 131.0 LDPC Encoder and Decoder

CCSDS 131.0 AR4JA LDPC Encoder and Decoder

CCSDS 231.0 LDPC Encoder and Decoder

DVB-S2X Demodulator

DVB-S2X LDPC and BCH Decoder

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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